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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANTS

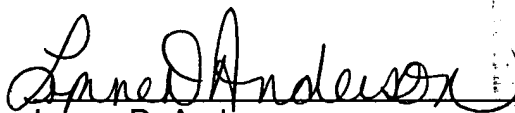
Ex parte FUJII

EXHAUST EMISSION CONTROL SYSTEM  
FOR AN INTERNAL COMBUSTION ENGINE

Serial Number: 09/674,522  
Filed: January 2, 2001  
Appeal No.:  
Group Art Unit: 3514  
Examiner: J. Nguyen

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Respectfully submitted,

  
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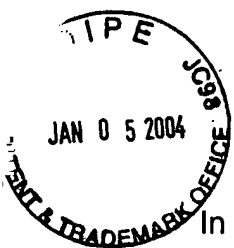
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of:

Takehiro FUJII

Application No.: 09/674,522

Filed: January 2, 2001

For: CHIP TYPE EMITTING DEVICE

Art Unit: 3514

Examiner: J. Nguyen

Attorney Dkt. No.: 107400-00017

BRIEF ON APPEAL

I. INTRODUCTION

This is an appeal from the action of the Examiner dated June 9, 2003, finally rejecting claims 1-5 as being unpatentable over certain prior art under 35 U.S.C. §103. A Notice of Appeal was timely filed on September 9, 2003.

II. REAL PARTY IN INTEREST

The real party in interest in present application on appeal is ROHM CO., LTD., 21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto-shi, Japan, by virtue of an Assignment recorded in the U.S. Patent and Trademark Office on January 2, 2001 at Reel 011445, Frame 0787.

III. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellant's representative or Assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

#### IV. STATUS OF CLAIMS

Claims 1-5 are being appealed. Claim 1 is independent. Claims 2-5 depend directly or indirectly from claim 1. The claims on appeal are set forth in the attached Appendix I.

#### V. STATUS OF AMENDMENTS

All Amendments have been entered.

#### VI. SUMMARY OF THE INVENTION

##### A. Summary

The present invention is directed to a construction for downsizing a chip type light emitting device in which an LED chip is mounted on a substrate to form a pair of electrodes at both ends of the substrate, and at the same time the electrodes are conducted on a rear surface of the substrate so that the substrate can be directly connected to a circuit board when it is mounted thereto.

Under a condition by which downsizing of a chip type light emitting device is needed, it is required that an LED chip is displaced from the substrate center as shown in Fig. 3 of Appellant's specification. But displacing the LED chip can create a problem of degrading light emitting patterns, and when the LED chip is arranged at the center portion of the substrate, as shown in Fig. 4 of Appellant's specification, there is simply no place to carry out wire bonding. Moreover, on the notch where the electrode pattern is allowed, a pressing force cannot be sufficiently applied when the wire-bonding is carried out ultrasonically, hence causing a problem for obtaining a reliable bonding.

In sum, the present invention is characterized such that a notch on the second electrode pattern side is divided into two, and the two notches are formed in such a way that a space for wire bonding can thereby be secured between the notches.

#### B. The Claimed Invention

Appellant's independent claim 1 recites a chip type light emitting device including, a board of nearly rectangular shape in a plane view. First and second electrode patterns are formed at both ends in a longitudinal direction of a surface of the board. A light emitting diode (LED) chip is mounted on the first electrode pattern. A metal wire is connected to the LED chip and the second electrode pattern by wire bonding and a translucent resin mold which seals the LED chip and the metal wire. One notch is formed at one end of the board at the first electrode pattern side and two notches are formed at both sides of the other end of the board at the second electrode pattern side. Each of the electrode patterns is formed so as to cover the one notch or two notches through an entire width of the board, and the positions at both ends of the translucent resin mold are arranged to the positions at both ends in a longitudinal direction of the board.

#### VII. THE FINAL REJECTION

Claims 1-5 are pending in this application. Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 3 or 4 of the acknowledged prior art ("APA") in view of JP 49-48267 ("JP '267"). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Figs. 3 or 4 of APA, as modified by JP '267, in further view of Okazaki, U.S. Patent No. 5,814,837.

### VIII. ISSUES ON APPEAL

The issues on appeal are whether:

(A) Claims 1, 2, 4 and 5 are unpatentable under 35 U.S.C. § 103 over APA in view of JP '267.

(B) Claim 3 is unpatentable under 35 U.S.C. § 103 over APA, as modified by JP '267, and further in view of Okazaki.

### IX. GROUPING OF CLAIMS

Each claim of this patent application is separately patentable, and upon issuance of a patent, will be entitled to a separate presumption of validity under 35 U.S.C. § 282. For convenience in the handling of this appeal, the claims are grouped as follows:

Group I, independent claim 1 and dependent claims 2, 4 and 5.

Group II, dependent claim 3.

Each of the Groups I-II will be argued separately in the following arguments. The Groups do not stand or fall together.

### X. APPELLANT'S ARGUMENTS

#### The Law

In order to be unpatentable under 35 U.S.C. § 103, several basic factual inquiries must be made to determine obviousness or non-obviousness of the patent application claims. These factual inquiries are set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 U.S.P.Q. 459, 467 (1996):

Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; the

level of ordinary skill in the pertinent art resolved.  
Against this backdrop, the obviousness or non-obviousness of the subject matter is determined.

Also, as stated by the Federal Circuit in *In re Ochiai*, 37 U.S.P.Q. 2d 1127, 1131 (Fed. Cir. 1995):

[t]he test of obviousness vel non is statutory. It requires that one compare the claim's subject matter as a whole with a prior art to which the subject matter pertains. 35 U.S.C. § 103.

The inquiry is highly fact-specific by design.... When the references cited by the Examiner fail to establish a prima facie case of obviousness, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). (Emphasis added.)

When rejecting claims under 35 U.S.C. § 103, an Examiner bears an initial burden of presenting a prima facie case of obviousness. A prima facie case of obviousness is established only if the teachings of the prior art would have suggested the claimed subject matter to a person of ordinary skill in the art. If an Examiner fails to establish a prima facie case, the rejection is improper and will be overturned. See: *In re Rijckaert*, 9 F.3d 1531, 28 U.S.P.Q. 2d. 1955 (Fed. Cir. 1993). "If examination... does not produce a prima facie case of unpatentability, then without more the applicant is entitled to the grant of the patent." *In re Oetiker*, 977 F.2d 1443, 1445-1446 24 U.S.P.Q. 2d. 1443, 1444 (Fed. Cir. 1992).

A. REJECTION OF CLAIMS 1, 2, 4 AND 5 UNDER 35 U.S.C. § 103(a)

Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Figure 3 or 4 of the acknowledged prior art ("APA") in view of JP 49-48267 ("JP '267").

The Office Action takes the position that APA discloses all the elements of the claimed invention, with the exception of disclosing two notches being formed at both sides of the other end of the board at the second electrode pattern side. JP '267 is cited for disclosing this limitation. However, Appellants submit that claims 1, 2, 4 and 5 recite subject matter that is neither disclosed nor suggested by any combination of the prior art.

In making this rejection, the Final Office Action takes the position that the combination of APA and JP '267 discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, in the chip type light emitting device of the present invention, one notch is formed at one end of the board at the first electrode pattern side and two notches are formed at both sides of the other end of the board at the second electrode pattern side, each of the electrode patterns is formed so as to cover the one notch or two notches through an entire width of the board, and the positions at both ends of the translucent resin mold are arranged to the positions at both ends in a longitudinal direction of the board.

As a result of the claimed configuration, one notch is formed at one end of the board and two notches are formed at the other end so that the polarity of the LED chip can be checked easily. If the translucent resin mold is milk white, the LED chip embedded in the translucent resin mold is illegible. Thus, in the present invention, one notch is formed at one end of the board and two notches are formed at the other end.

Therefore, because the electrode structure is asymmetric, the polarity can be checked easily because of the structure of the chip type light-emitting device.

Additionally, the positions of both ends of the translucent resin mold are arranged at the positions of both ends in a longitudinal direction of the board. Thus, the contact area for picking up the board can be increased and the handling process can be performed smoothly for an ultra small-sized chip type light emitting device.

### 1. Summary of JP 49-48267

As shown in Fig. 2 of JP '267, the same insulation substrates 1b and 1c are laminated on both ends of one of the main surfaces of insulation substrate 1a, respectively, via metallized layers L1 and L2, and are formed in a U-letter shape. Metallized layers 2a, 2b and 2c are disposed on the flat section of the relevant top substrate surfaces, and are distantly separated and electrically insulated by the inner side surface sections of substrates 1b and 1c. An electronic device (for example, a semiconductor device) 3 is placed on metallized layer 2a of the top surface of substrate 1a, which corresponds to a grooved section of the U-letter shape insulation substrate, and one of the derived electrodes is electronically and thermally connected to metallized layer 2d provided on the other main surface (rear surface) of insulation substrate 1a via metallized layer 2a and a metallized layer of notched portion 4. In addition, two other derived electrodes of electronic device 3 are connected to metallized layers 2b and 2c, respectively, via metal wire 5, and are electrically and thermally connected to two metallized layers 2e and 2f, respectively, which are disposed on the other main surface of the same insulation substrate 1a via metallized layers 3b, 3a or 3c, 3'a of the outer



side surface section of the substrate. The electrodes are mutually insulated from metallized layer 2d.

The Final Office Action dated June 9, 2003 asserts that it would have been obvious for one of ordinary skill in the art to modify the APA to include the two notches, as taught by JP '267, for the purpose of reducing the size of the LED device. However, it is respectfully submitted that there is simply no motivation to combine APA with JP '267, and that the combination thereof would not have yielded the claimed invention.

In the "Response to Arguments" Section, the Final Office Action takes the position that in JP '267, two notches are clearly provided at the same substrate end 1a of the second electrode pattern side 1b, 1c. However, electronic device 3 of JP '267 is a three-terminal electronic device such as a transistor, and has three electrodes. The electrodes formed on the top surface side are denoted 2b, 2c, and are connected to electronic device 3 by wire 5. The notches provided at the end section are disposed one each only on the relevant sides of the different electrodes 2b, 2c, respectively. Therefore, JP '267 fails to disclose or suggest that one notch is formed at one end of the board at the first electrode pattern side and that two notches are formed at both sides of the other end of the board at the second electrode pattern side, as recited in Appellant's claim 1. In addition, because the electronic device of JP '267 has three electrodes, such a device cannot be an LED, which has two electrodes.

In the "Response to Arguments" Section, the Final Office Action states that the LED chip in Fig. 3 of the APA is almost centered. However, Appellant's specification at lines 5-11 of page 5 clearly discusses that the LED chip 1 is mounted at an off-centered position on board 2. Therefore, as shown in Fig. 3 of the APA, the LED chip 1 cannot

be centered on board 2. As a result, LED 1 is also located at a decentered position on translucent resin mold 6. Thus, as shown in the luminous intensity characteristics diagram of Fig. 5 of the APA, this creates a problem because the luminous intensity distribution cannot be obtained in the longitudinal direction of board 2. Thus, APA's construction in Fig. 3 lacks any LED chip at the substrate center, and therefore a combination thereof with JP '267 would not have yielded the present invention as set forth in claim 2.

Furthermore, JP '267 merely describes a protective layer W and does not mention a covering with transparent resin. Accordingly, JP '267 is not at all concerned with the wire bonding between two notches to secure a place for bonding. Instead, JP '267 merely discloses a construction by which corners are removed. As such, without using impermissible hindsight, one skilled in the art would lack any motivation to modify APA in view of JP '267 for the purpose of downsizing the chip type light-emitting device in order to arrive at the claimed invention.

However, *assuming arguendo*, even if one skilled in the art were to combine APA and JP '267, one would not have arrived at the claimed invention, which advantageously downsizes a chip type light emitting device by dividing a notch into two on one end of the substrate, which is the second electrode pattern side, and forming the two notches on both sides (width direction) so that wire-bonding between the divided notches can be carried out.

As such, Appellants respectfully submit that the requisite suggestion or motivation in either of the references to modify and/or combine the references as alleged in the Office Action is absent. Both references, even combined, fail to teach or

suggest all of the claimed features of Appellant's recited invention. Additionally, the teaching or suggestion to make the alleged modification and/or combination is absent from the references and only found in the Appellant's disclosure. Accordingly, Appellant respectfully submits that the Examiner has failed to establish a prima facie case of obviousness as outlined by 35 U.S.C. § 103, MPEP § 706.02(j).

In other words, Appellant strongly, but respectfully, submits that the only teaching or suggestion of the claimed structural features exist in Appellant's own disclosure. The Office Action is attempting to improperly use hindsight, based on the teachings in the Appellant's disclosure, to say that it would have been obvious to combine APA with JP '267 to arrive at the claimed invention.

In addition, MPEP § 2143 also states that the prior art must contain some motivation or incentive to modify and/or combine references in such a way as to yield the claimed invention. Although the motivation or incentive does not need to be explicit in a cited reference, it must be inherent. There is no such suggestion or motivation explicit or inherent.

In sum, as discussed above, the combination of APA and JP '267 fails to disclose a chip type light emitting device comprising: a board of nearly rectangular shape in a plane view; first and second electrode patterns formed at both ends in a longitudinal direction of a surface of said board; a light emitting diode (LED) chip mounted on said first electrode pattern; a metal wire connected to said LED chip and said second electrode pattern by wire bonding; and a translucent resin mold which seals said LED chip and said metal wire; wherein one notch is formed at one end of said board at said first electrode pattern side and two notches are formed at both sides of the other end of

said board at said second electrode pattern side, each of said electrode patterns is formed so as to cover said one notch or two notches through an entire width of said board, and the positions at both ends of said translucent resin mold are arranged to the positions at both ends in a longitudinal direction of said board, as recited in Appellant's claim 1.

Therefore, Appellant respectfully submits that the Examiner has not made a prima facie rejection under 35 U.S.C. § 103(a) because the applied prior art references cited fail to teach or suggest each element of the presently claimed invention, as set forth in claim 1.

As claims 2, 4 and 5 depend directly or indirectly from claim 1, Appellant respectfully submits that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least same reasons as discussed above.

B. REJECTION OF CLAIM 3 UNDER 35 U.S.C. § 103(a)

Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over APA as modified by JP '267 and in further view of Okazaki. In making this rejection, the Final Office Action took the position that the combination of APA and JP '267 discloses all the elements of the claimed invention, except the board size being 1.6 mm X 0.8 mm or less. Okazaki is cited for disclosing this limitation.

2. Summary of Okazaki

Okazaki discloses a compact LED with a sealing member. The LED includes an insulating substrate having a plurality of through holes. A p-side semiconductor layer

and an n-side semiconductor layer are joined into an p-n junction and are placed between each pair of adjacent through holes.

The Final Office Action asserts that Okazaki teaches a substrate 17 which is 1.6 mm x 0.8 mm or smaller, and when combined with the teaching of Fig. 3 or Fig. 4 of the APA, would be sufficient to yield the present invention as set forth in claim 3. However, it is respectfully submitted that there is simply no motivation for such a suggested combination by one skilled in the art because the device construction of Okazaki, other than the dimensions of the substrate in Okazaki, is completely different from either the APA or claimed invention. Okazaki is not at all concerned with securing a space for wire bonding when the device is down-sized. As such, one skilled in the art would simply not be able to carry out wire bonding using the substrate of Okazaki.

Even if a chip size similar to that in claim 3 is disclosed in Okazaki, the APA is an LED which has a construction completely different from Okazaki, and it is obvious to those skilled in the art that even if a small substrate is disclosed in a different construction, The techniques of the different constructions cannot be combined and there is no motivation to combine them. Thus, Okazaki fails to rectify the deficiencies of AP, as modified by JP '267.

Still further, Appellant's specification clearly discusses at page 2, line 22 – page 3, line 6, that a problem with the prior art is that when the board is 1.6 mm x 0.8 mm or smaller, handling cannot be performed smoothly. Additionally, at page 4, lines 8-12 of Appellant's specification, it is discussed that another problem with the prior art is that if the board size is 1.6 mm x 0.8 mm or smaller, the LED chip cannot be centered on the board. As Appellant's specification demonstrates that the board size has a specific

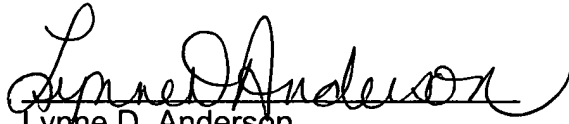
purpose, the range of 1.6 mm x 0.8 mm or smaller is not merely design choice.

For all of the above noted reasons, it is strongly contended that certain clear differences exist between the present invention as claimed in claims 1-5 and the prior art relied upon by the Examiner.

This final rejection being in error, therefore, it is respectfully requested that this honorable Board of Patent Appeals and Interferences reverse the Examiner's decision in this case and indicate the allowability of application claims 1-5.

In the event that this paper is not being timely filed, the Appellant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees which may be due with respect to this paper may be charged to our Deposit Account No. 01-2300, referencing docket number 107400-00017.

Respectfully submitted,

  
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## APPENDIX 1

### CLAIMS ON APPEAL

1. (Previously Presented) A chip type light emitting device comprising:  
a board of nearly rectangular shape in a plane view;  
first and second electrode patterns formed at both ends in a longitudinal direction of a surface of said board;  
a light emitting diode (LED) chip mounted on said first electrode pattern;  
a metal wire connected to said LED chip and said second electrode pattern by wire bonding; and  
a translucent resin mold which seals said LED chip and said metal wire;  
wherein one notch is formed at one end of said board at said first electrode pattern side and two notches are formed at both sides of the other end of said board at said second electrode pattern side, each of said electrode patterns is formed so as to cover said one notch or two notches through an entire width of said board, and the positions at both ends of said translucent resin mold are arranged to the positions at both ends in a longitudinal direction of said board.
2. (Original) The chip type light emitting device of claim 1, wherein said LED chip is almost centered on said board.
3. (Original) The chip type light emitting device of claim 1, wherein said board size is 1.6 mm x 0.8 mm or less.
4. (Previously Presented) The chip type light emitting device of claim 1, wherein said metal wire is connected to said LED chip and the surface of said second



electrode pattern, which is located on a portion of said board between said two notches formed at both sides of the other end of said board at said second electrode pattern side, by wire bonding.

5. (Original) The chip type light emitting device of claim 1, wherein said one notch formed at said one end of said board at said first electrode pattern side is semi-cylindrical and said two notches formed at both sides of the other end of said board at said second electrode pattern side are quarter-cylindrical.